REMARKS

Claims 6, 10-12, 15 and 16 are pending. Claim 13 is canceled and claims 6 and 10 are amended. A marked-up version showing the changes made by the present amendment is attached hereto as "**Version with markings to show changes made**."

As a preliminary matter, the paragraph bridging pages 2 and 3 of the Office Action has been noted with respect to the changes made to 35 U.S.C. §102(e) by the American Inventors Protection Act of 1999. The Examiner asserts that the changes do not apply to the present application since it was not "filed on or after November 29, 2000." However, it is respectfully submitted that the changes do apply to the present application since a continued prosecution application was filed on January 9, 2002.

Claim 13 was objected to under 37 C.F.R. §1.75(c), as failing to limit the subject matter of the previous claim. Accordingly, claim 13 has been canceled.

Claim 10 was rejected under 35 U.S.C. §102(e) as being anticipated by Hause et al. This rejection is respectfully traversed.

Hause et al., is silent about the feature of claim 10 in which the gate oxide film is left on the substrate after patterning the gate electrode, and nitrogen atoms are introduced into the part of the gate oxide film not covered by the gate electrode. See Fig. 4 of the present application. In Hause et al., there is no gate oxide film exposed to allow the introduction of nitrogen atoms into the gate oxide film while using the gate electrode pattern as a mask. Furthermore, Hause et al. does not appear to teach or suggest introducing N atoms, after the step of introducing the impurity element. Accordingly, Hause et al. fails to anticipate claim 10.

Claims 6 and 13 were rejected under 35 U.S.C. §103(a) as being unpatentable over Hause et al. in view of Bhat et al. This rejection is respectfully traversed.

With respect to claim 6, Hause et al. does teach or suggest introducing N atoms into the gate oxide film or using the gate electrode pattern as a mask, as noted above. Bhat et al. is also silent about introducing nitrogen atoms into the part of the gate oxide film remaining on the substrate outside the gate electrode pattern. Accordingly, claims 6 and 13 are patentable over the combination of Hause et al. and Bhat et al.

Claims 11 and 12 were rejected under 35 U.S.C. §103(a) as being unpatentable over Hause et al. in view of Arai et al. This rejection is respectfully traversed.

Arai et al. fails to provide the teachings in which Hause et al. lacks. That is, Arai et al. fails to teach or suggest introducing N atoms into the gate oxide film or using the gate electrode pattern as a mask. As noted above, independent claim 10 requires that the gate oxide film remains on the substrate after patterning of the gate electrode in the present invention.

Claims 6 and 13 were rejected under 35 U.S.C. §103(a) as being unpatentable over Tseng et al. in view of Bhat et al. Favorable reconsideration of this rejection is earnestly solicited.

Tseng et al. teaches a structure having a multilayer gate dielectric film (13-16). In Tseng et al., it is noted that there is an interface layer (13) of silicon oxynitride between a substrate (base layer) (12) and a thermal oxide film (14), wherein there is further provided a porous dielectric film (16) between the thermal oxide film (14) and the gate electrode (20). In Tseng et al., nitrogen atoms are introduced after forming the gate electrode (20) by a thermal annealing process, wherein the nitrogen atoms thus introduced are "piled up" to form the interface layer. See column 3, line 30 of

Tseng et al.

Contrary to Tseng et al., the nitrogen atoms are introduced so as to terminate the dangling bonds formed in the thermal oxide film forming the gate electrode at the time of patterning of the gate electrode, in view of the fact that the gate electrode is formed in direct contact with the gate oxide film in the case of the present invention and the patterning of the gate electrode by a dry etching process caused damaging of the gate oxide film exposed at both sides of the gate electrode pattern.

In the case of Tseng et al., the thermal oxide film does not make a direct contact with the gate electrode and thus experiences no damaging at the time of the patterning of the gate electrode. Further, Tseng et al. intentionally causes a concentration of nitrogen atoms at the interface of the substrate and the gate insulation film, while this teaches away from the present invention.

Claims 10-13 were rejected under 35 U.S.C. 103(a) as being unpatentable over Tseng et al. in view of Arai et al. Arai et al. is relied upon by the Examiner for its teachings directed to implanting nitrogen in a gate oxide. Favorable reconsideration of this rejection is earnestly solicited.

Claim 10 has been amended to specify that the gate electrode pattern is in direct contact with the gate oxide film. The combination of art fails to teach or suggest the features of amended claim 10.

For at least the foregoing reasons, the claimed invention distinguishes over the cited art and defines patentable subject matter. Favorable reconsideration is earnestly solicited.

Should the Examiner deem that any further action by Applicant would be desirable to place the application in condition for allowance, the Examiner is encouraged to telephone Applicant's

undersigned attorney.

In the event that this paper is not timely filed, Applicant respectfully petitions for an appropriate extension of time. Please charge any fees for such an extension of time and any other fees which may be due with respect to this paper, to Deposit Account No. 01-2340.

Respectfully Submitted,

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Enclosures: Version with markings to show changes made
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VERSION WITH MARKINGS TO SHOW CHANGES MADE 09/428,052

IN THE CLAIMS:

Please amend claims 6 and 10 as follows:

6. (Four Times Amended) A method of fabricating a semiconductor device, comprising the steps of:

forming a gate oxide film on a substrate by a thermal oxide film;

forming a gate electrode pattern on said gate oxide film;

forming diffusion regions in said substrate at both lateral sides of said gate electrode pattern by introducing an impurity element into said substrate through said gate oxide film while using said gate electrode pattern as a mask; and

introducing N atoms into said gate oxide film while using said gate electrode pattern as a mask,

said step of introducing said impurity element being conducted prior to said step of introducing N atoms into said gate oxide film,

wherein said step of introducing N atoms into said gate oxide film comprises a thermal annealing process of said gate oxide film conducted in an atmosphere containing NO,

wherein activation of said impurity element is conducted simultaneously to said thermal annealing process,

said thermal annealing process being conducted at a temperature of about 800°C.

10. (Five Times Amended) A method of fabricating a semiconductor device, comprising the steps of:

forming a gate oxide film on a substrate by a thermal oxide film;

forming a gate electrode pattern on said gate oxide film such that said gate electrode pattern is in direct contact with said gate oxide film;

forming diffusion regions in said substrate at both lateral sides of said gate electrode pattern by introducing impurity element into said substrate through said gate oxide film while using said gate electrode pattern as a mask; and

introducing N atoms, after said step of introducing said impurity element, into said gate oxide film while using said gate electrode pattern as a mask,

wherein said step of introducing N atoms into said gate oxide film includes an ion implantation process of N ions.